US-PAT-NO: 6470048

DOCUMENT-IDENTIFIER: US 6470048 B1

TITLE: Frequency-based
video data substitution for increased
                              video compression
ratios

---------- KWIC ----------

Abstract Text - ABTX (1):
    Frequency information is selectively
removed from a video signal in order to
decrease the number of color values
required for video compression. Removal of
the frequency information includes both
periodic raking out of narrow frequency
bands, and **rounding of frequency** values.
The frequency information removal is
carried out selectively in those portions
of the visible light spectrum in
which the human eye's color response is
strongest, thus allowing increases in
video compression ratios without visible
degradation of image quality.

Detailed Description Text - DETX (14):
    Similarly, the compressor/encoder used
need not be an MPEG encoder. The

present invention may be used with any compression mechanism which will benefit from the removal from the incoming data of information so as to reduce the number of data values which must be stored, manipulated, and/or transmitted. Nor is it necessary that the signal be a video signal; the signal may be any signal whose compression ratio may be increased by the selective removal of information which will not noticeably degrade the accuracy of data reproduction. It will also be appreciated that in the data removal such as the data raking and data rounding illustrated herein, the exact parameters for the raking and rounding are somewhat arbitrary, and are subject to experimental determination of acceptable or optimal parameters given system performance requirements such as maximum data bit rate, computational throughput rate, image quality, and the like. For example, although the raking is described as being performed periodically, it is not necessary that the wavelength intervals between raking lines be consistent or that the raking lines have uniform width. Such variations are intended as being within the scope of the term **"periodic"**.

US-PAT-NO: <u>**6233672**</u>

DOCUMENT-IDENTIFIER: US <u>**6233672**</u> B1
See image for Certificate of Correction

TITLE: Piping <u>**rounding**</u> mode
bits with floating point
                              instructions to
eliminate serialization

---------- KWIC ----------

Abstract Text - ABTX (1):
   A floating point unit is provided which
conveys the <u>**rounding**</u> mode in effect
upon dispatch of a particular instruction
with that particular instruction into
the execution pipeline of the floating
point unit. Upon dispatch of a control
word update instruction into the execution
pipeline, the <u>**rounding**</u> mode is
updated according to the updated control
word provided for the control word
update instruction. Instructions
subsequent to the control word update
instruction thereby receive the updated
<u>**rounding**</u> mode as those instructions are
dispatched. The updated <u>**rounding**</u> mode is
available to the subsequent
instructions prior to retiring the control
word update instruction. The

rounding mode is therefore updated without serializing the update. If the control word update instruction modifies the value in a field other than the **rounding** mode, the instructions subsequent to the control word update instruction may be discarded and re-executed subsequent to updating the control word register with the updated control word. In this manner, the control word update is effectively serialized for cases in which a field other than the **rounding** mode is updated.

US Patent No. - PN (1):
   6233672

US Document Identifier - DID (1):
   US **6233672** B1

TITLE - TI (1):
   Piping **rounding** mode bits with floating point instructions to eliminate serialization

Brief Summary Text - BSTX (3):
   This invention relates to the field of microprocessors and, more particularly, to the handling of **rounding** modes within floating point units of

microprocessors.

Brief Summary Text - BSTX (9):
   Floating point data types produce
challenges for the microprocessor
designer. For example, an arithmetic
operation between two floating point
numbers may produce a value which is within
the floating point numerical range,
but cannot be exactly represented within
the floating point data type format.
Therefore, the result must be **rounded** to a
representable number. Generally
speaking, **rounding** refers to selecting a
number which is representable in the
target data type format (e.g. single,
double, or extended precision) to be the
result of a calculation in place of the
exact result when the exact result is
not representable in the target data
format. The **rounding** may be accomplished
in a number of ways. For example, the
result can be truncated to fit in the
target data format. Alternatively, the
nearest representable number to the
actual result may be chosen (whether that
number is numerically higher or lower
than the actual result). Additional
alternative **rounding** modes include
rounding up to a numerically larger number,
or **rounding** down to a numerically
smaller number. Many other types of
rounding modes may be used, including
rounding to a lesser precision (i.e. fewer

bits of significand), etc.

Brief Summary Text - BSTX (10):
    Instead of choosing only one **rounding**
mode, which may not serve the needs of
all users, microprocessors typically allow
the user to select the **rounding**
mode. A control word is defined for the
microprocessor, and a field within the
control word comprises the **rounding** mode.
A special control word update
instruction is provided to allow the user
to update the control word, including
the **rounding** mode. Generally speaking, the
control word stores a number of
fields regarding the operating state of the
floating point unit. A precision
control field may be included, indicating
the precision of the results (single,
double, or extended). Additionally,
exception masking may be stored in the
control word. Floating point calculations
can produce a variety of exceptions
(i.e. conditions which may require
corrective action such as discarding the
instruction stream and refetching or
trapping to a software routine for
diagnosis). If a particular exception is
unimportant to a particular user,
then that exception can be masked in the
control word.

Brief Summary Text - BSTX (12):

Unfortunately, certain algorithms rely
on repeatedly changing the **rounding**
mode of the floating point unit. For
example, interval arithmetic is often
used to compute an upper and lower bound of
a correct result, given that the
exact result often cannot be represented.
For interval arithmetic, the
rounding mode is different when computing
the upper bound than when computing
the lower bound. Therefore, the
performance of interval arithmetic suffers
because changing the **rounding** mode causes
serialization. Other algorithms
which change the **rounding** mode often
similarly suffer performance degradation.

Brief Summary Text - BSTX (14):
    The problems outlined above are in large
part solved by a floating point
unit in accordance with the present
invention. The floating point unit conveys
the **rounding** mode in effect upon dispatch
of a particular instruction with that
particular instruction into the execution
pipeline of the floating point unit.
Upon dispatch of a control word update
instruction into the execution pipeline,
the **rounding** mode is updated according to
the updated control word provided for
the control word update instruction. Each
instruction receives a copy of the
rounding mode appropriate at the time of
issue of that instruction. For

example, in an in-order embodiment of a
floating point unit, instructions
subsequent to the control word update
instruction receive the updated **rounding**
mode as those instructions are dispatched.
Advantageously, the updated
rounding mode is available to the
subsequent instructions prior to completion
of the control word update instruction.
The **rounding** mode is therefore updated
without serializing the update.
Advantageously, applications which change
the
rounding mode often may experienced
increased performance due to the lack of
serialization upon **rounding** mode updates.

Brief Summary Text - BSTX (15):
    If the control word update instruction
modifies the value in a field other
than the **rounding** mode, the instructions
subsequent to the control word update
instruction may be discarded and
re-executed subsequent to updating the
control
word register with the updated control
word. In this manner, the control word
update is effectively serialized for cases
in which a field other than the
rounding mode is updated. The control word
update instruction may provide the
updated control word in a number of
manners. For example, the updated control
word may be an immediate field of the

control word update instruction.
Alternatively, the updated control word may
be implicit in the opcode of the
instruction or may be a memory or register
operand.

Brief Summary Text - BSTX (16):
   Broadly speaking, the present invention
contemplates a floating point unit
for a microprocessor comprising an
execution pipeline and a **rounding** mode
storage. Coupled to the execution
pipeline, the **rounding** mode storage is
configured to store a **rounding** mode
indicative of a type of **rounding** to be
applied to results of floating point
instructions. The execution pipeline is
configured to convey the **rounding** mode
along with a particular instruction
dispatched into the execution pipeline.
Additionally, the execution pipeline
is configured to **round** a particular result
corresponding to the particular
instruction according to the **rounding** mode.

Brief Summary Text - BSTX (17):
   The present invention further
contemplates a method for performing
rounding
in a floating point unit. A current
rounding mode is conveyed with a floating
point instruction into an execution
pipeline of the floating point unit.   The

current **rounding** mode is updated to an
updated **rounding** mode upon dispatch of a
control word update instruction into the
execution pipeline. The updating is
performed in a non-serialized manner.

Brief Summary Text - BSTX (18):
    The present invention still further
contemplates a microprocessor comprising
a floating point unit and a reorder buffer.
 The floating point unit includes
an execution pipeline into which the
floating point unit is configured to
convey a **rounding** mode along with each
instruction. Additionally, the floating
point unit is further configured to update
the **rounding** mode in response to a
control word update instruction without
serialization. Coupled to the floating
point unit, the reorder buffer is
configured to process instruction
exceptions.
Furthermore, the reorder buffer is further
configured to convey a cancel
indication to the floating point unit if
one or more floating point
instructions are canceled in response to
one of the instruction exceptions.

Drawing Description Text - DRTX (7):
    FIG. 5 is a diagram of portions of a
first embodiment of the floating point
unit shown in FIG. 4, illustrating the

handling of the **rounding** mode.

Drawing Description Text - DRTX (8):
   FIG. 6 is a diagram of portions of a
second embodiment of the floating point
unit shown in FIG. 4, illustrating an
alternative handling of the **rounding**
mode.

Drawing Description Text - DRTX (9):
   FIG. 7 is a flowchart of the operation
of a control unit configured to
handle **rounding** mode updates shown in FIGS.
5 or 6, according to one embodiment
of the control unit.

Detailed Description Text - DETX (5):
   Generally speaking, FPU 36 is configured
to execute floating point
instructions. FPU 36 includes an execution
pipeline for executing the
instructions. Along with conveying the
instructions through the execution
pipeline, FPU 36 also conveys the **rounding**
mode relevant to the instructions.
If a control word update instruction is
detected, an updated **rounding** mode from
the updated control word supplied for the
control word update instruction is
noted by FPU 36 when the control word
update instruction is dispatched into the
instruction processing pipeline.

Instructions subsequent to the control word update instruction receive the updated **rounding** mode as the subsequent instructions are dispatched into the execution pipeline. Advantageously, the control word update instruction is not serialized. Performance of instruction code sequences which update the **rounding** mode often may thereby be increased. If, upon retiring the control word update instruction and updating the control word of FPU 36, other fields of the control word besides the **rounding** mode are updated, the instructions subsequent to the control word update instruction can be discarded and reexecuted.

Detailed Description Text - DETX (6):

The copy of the **rounding** mode noted by FPU 36 is updated to the current **rounding** mode stored in the control word upon cancellation of a control word update instruction from the execution pipeline. In this manner, the copy of the **rounding** mode is resynchronized to the current **rounding** mode after being erroneously updated. When the control word update instruction is canceled from the execution pipeline, the instructions subsequent to the control word update instruction within the execution pipeline are also canceled or are to be canceled in a subsequent clock cycle. Therefore, correcting the copy of the

rounding mode is sufficient for correcting
the effects of pipelining the
rounding mode with each instruction.

Detailed Description Text - DETX (59):
   FPU environment 88 stores control and
status information regarding the state
of FPU 36. A control word may be stored
which indicates the **rounding** and
precision modes of FPU 36 as well as a mask
for various floating point
exceptions. A status word may also be
stored which indicates which floating
point exceptions have been detected, the
top of stack pointer, etc.

Detailed Description Text - DETX (61):
   Turning next to FIG. 5, portions of a
first embodiment of FPU 36 are shown
illustrating the conveyance of a **rounding**
mode with each instruction through
the execution pipeline of FPU 36. FPU
control unit 92, FPU core 94, FPU
environment 88, and assembly queue 80 are
shown. A first entry of assembly
queue 80 is illustrated via an opcode
storage 110, a register specifier storage
112, and a memory operand storage 114.
Similar opcode storage, register
specifier storage, and memory operand
storage locations are included in
assembly queue 80 for storing other
instructions. Additionally, assembly queue

80 includes a control unit 116 and a
rounding mode storage 118. FPU
environment 88 includes a control word
register 120. Additionally, several
pipeline stages 122A-122D are illustrated
within FPU control unit 92. Each
pipeline state 122A-122D includes a field
124 for storing instruction
information (e.g. opcode, operand
information, etc.) and a field 126 for
storing the **rounding** mode applicable to the
instruction. FPU core 94 includes
a pipeline as well, and as an alternative
to storing the **rounding** mode in FPU
control unit 92, the **rounding** mode may be
pipelined within FPU core 94.
Control unit 116 is coupled to **rounding**
mode storage 118 and to opcode storage
110. Furthermore, control unit 116
receives a cancel CW update signal upon a
conductor 128. **Rounding** mode storage 118
is further coupled to memory operand
storage 114 and to control word register
120. Furthermore, **rounding** mode
storage 118 is coupled to a first pipeline
stage 122A. It is noted that,
although portions of the internal circuitry
of FPU control unit 92, FPU
environment 88, and assembly queue 80 are
shown in FIG. 5, additional internal
circuitry (not shown) may be employed by
each block for other functions.

Detailed Description Text - DETX (62):

Rounding mode storage 118 stores the rounding mode for FPU 36 which reflects the execution of any control word update instructions which have previously been executed, including any control word update instructions which are outstanding within the execution pipeline. Therefore, the rounding mode stored in rounding mode storage 118 may differ from the rounding mode stored in control word register 120 during clock cycles in which a control word update instruction is outstanding within the execution pipeline. As instructions are dispatched from assembly queue 80 into the execution pipeline, the rounding mode stored in rounding mode storage 118 is dispatched as well. As the instruction flows through pipeline stages 122, the corresponding rounding mode is carried along as well. When an instruction reaches the pipeline stage in which rounding is performed, the pipelined rounding mode is used to control the rounding.

Detailed Description Text - DETX (63):
According to one embodiment, the rounding mode comprises two bits. The two bits are encoded to select one of four possible rounding modes. A rounding mode encoding of `00` (binary) indicates that the rounding mode is round to nearest, in which the nearest representable

number (in absolute value) to the
precise result is selected as the **rounded**
result. A **rounding** mode encoding of
`01` indicates that the **rounding** mode is
round down (or **round** to negative
infinity), in which the precise result is
rounded to the next numerically
smaller representable value. A **rounding**
mode encoding of `10` indicates that
the **rounding** mode is **round** up (or **round** to
positive infinity), in which the
precise result is **rounded** to the next
numerically larger representable value.
Finally, a **rounding** mode encoding of `11`
indicates that the **rounding** mode is
truncate (or chop), in which the precise
result is truncated to the number of
significant bits which may be represented.

Detailed Description Text - DETX (64):
    Control unit 116 controls the update of
rounding mode storage 118. Control
unit 116 receives the opcode of the
instruction which is next to be dispatched
into the execution pipeline. If the
instruction is a control word update
instruction, then control unit 116 causes
the **rounding** mode portion of the
updated control word to be copied into
rounding mode storage 118 upon dispatch
of the control word update instruction. In
this manner, instructions
subsequent to the control word update
instruction receive the **rounding** mode

provided by the updated control word. According to one embodiment, the control word update instruction is defined to store a memory operand into control word register 120. Therefore, **rounding** mode storage 118 is coupled to receive the portion of the value stored in memory operand storage 114 which comprises the **rounding** mode when the corresponding instruction is a control word update instruction. Control unit 116 causes **rounding** mode storage 118 to store the field provided from memory operand storage 114 upon dispatch of the control word update instruction.

Detailed Description Text - DETX (65):

Control unit 116 also updates **rounding** mode storage 118 upon detection of a canceled control word update instruction. Control unit 116 is informed that a control word update instruction has been canceled via assertion of the cancel CW update signal. Control unit 116 causes **rounding** mode storage 118 to store the **rounding** mode provided by control word register 120 upon assertion of the cancel CW update signal. FPU control unit 92 may provide the cancel CW update signal, for example. FPU control unit 92 may assert the signal upon receiving a cancel indication from reorder buffer 32 and the instruction being canceled is a control word update instruction.

Alternatively, the cancel CW update signal may be asserted upon assertion of any cancel signal. The **rounding** mode would then be updated to the correct **rounding** mode if an update control word instruction were canceled, and the **rounding** mode would be updated to the same value that was stored in **rounding** mode storage 118 if the canceled instruction is not a control word update instruction. It is noted that, if the control word update instruction updates fields other than the **rounding** mode, then the execution pipeline is drained.

Detailed Description Text - DETX (67):

By conveying the **rounding** mode for each instruction with the instruction into the execution pipeline, FPU 36 may avoid serializing the update of the control word when only the **rounding** mode is to be updated. For applications in which changing the **rounding** mode is the most common reason for updating the control word, performance may be increased by the lack of serialization. Advantageously, **rounding** mode changes may be performed more often without serious performance degradation, allowing for applications which need to change the **rounding** mode often to achieve increased performance.

Detailed Description Text - DETX (68):

Turning now to FIG. 6, portions of a second embodiment of FPU 36 are shown illustrating the conveyance of a **rounding** mode with each instruction through the execution pipeline of FPU 36. FPU control unit 92, FPU core 94, FPU environment 88, and translate unit 82 are shown. Translate unit 82 includes a control unit 130 and a **rounding** mode storage 132. FPU environment 88 includes control word register 120, as shown in FIG. 6 above. Additionally, FPU control unit 92 includes several pipeline stages 122A-122D, each including a field 124 for storing instruction information (e.g. opcode, operand information, etc.) and a field 126 for storing the **rounding** mode applicable to the instruction. FPU core 94 includes a pipeline as well, and as an alternative to storing the **rounding** mode in FPU control unit 92, the **rounding** mode may be pipelined within FPU core 94. Control unit 130 is coupled to **rounding** mode storage 132. Control unit 130 receives a cancel CW update signal upon conductor 128, and further receives the opcode of the instruction being dispatched upon an opcode bus 134 from assembly queue 80. **Rounding** mode storage 132 is coupled to receive the **rounding** mode portion of the memory operand upon a memory operand bus 136 from assembly queue 80 and is further coupled to control word register

120. Furthermore, **rounding** mode storage
130 is coupled to a first pipeline
stage 122A.

Detailed Description Text - DETX (69):
   The embodiment shown in FIG. 6 locates
rounding mode storage 132 and the
associated control unit 130 within
translate unit 82. Accordingly, the opcode
and memory operand of the dispatching
instruction are conveyed to translate
unit 82 for detecting control word update
instructions and storing the **rounding**
mode portion of the updated control word
into **rounding** mode storage 132.
Similarly, control unit 130 is configured
to cause **rounding** mode storage 132 to
store the **rounding** mode portion of the
control word stored in control word
register 120 upon assertion of the cancel
CW update signal upon conductor 128.

Detailed Description Text - DETX (70):
   Turning next to FIG. 7, a flow chart
illustrating the operation of one
embodiment of control unit 116 (for the
embodiment shown in FIG. 5) or control
unit 130 (for the embodiment shown in FIG.
6) is shown. The control unit first
detects whether or not a canceled control
word update instruction has been
detected (decision block 140). If so,
then the **rounding** mode stored in the

rounding mode storage is copied from the control word stored in control word register 120 (step 142). If a canceled control word update instruction is not detected, then the control unit detects if a control word update instruction is being dispatched (decision block 144). If so, then the **rounding** mode stored in the **rounding** mode storage is updated from the updated control word provided as the memory operand of the control word update instruction (block 146). If neither a canceled control word update instruction nor a dispatching control word update instruction is detected, then the **rounding** mode stored in the **rounding** mode storage is left unmodified. As mentioned above, the **rounding** mode is conveyed into the execution pipeline along with each instruction.

Detailed Description Text - DETX (74):
    Multiplier stage 122B is used to perform multiplication of floating point numbers. Similarly, right shift stage 122C performs right shift operations. For example, right shift stage 122C may be used to perform the significand shift operation described above. Adder stage 122D performs the addition of floating point numbers. Count leading zeros stage 122E is used to count the leading zeros in the result significand, in order to place the result into

normal form (i.e. one binary one digit to the left of the decimal point). Left shifter stage 122F left shifts the significand according to the number of leading zeros provided by count leading zeros stage 122E, and adjusts the exponent accordingly. **Rounder** stage 122G **rounds** the result according to the **rounding** mode which was conveyed with the corresponding instruction. Finally, output fixup stage 122H is used to force the special encodings (zero, infinity, denormalized number, etc.) if the input operands or the result are special numbers. It is noted that, according to one embodiment, **rounder** stage 122G performs only the **rounding** of floating point numbers in accordance with the **rounding** mode conveyed with the instruction. It is noted than many other datapaths are possible. For example, the add and **round** operations may be performed in a single pipeline stage, etc.

Detailed Description Text - DETX (76):
    Turning now to FIG. 9, a diagram of a control word 160 which may be employed according to one embodiment of FPU 36 is shown. Control word 160 is the control word defined by the x86 microprocessor architecture. Control word 160 includes a pair of reserved fields 162 and 164. Generally, reserved fields 162

and 164 are ignored by FPU 36 and are
reserved for future expansion of control
word 160. A **rounding** mode field 166 is
included for storing the **rounding** mode.
Additionally, a precision control field 168
is included for defining the
precision mode of FPU 36. Precision
control field 168 may be encoded to
indicate single, double, or extended
precision. Finally, control word 160
includes an exception masks field 170. A
bit within exception masks field 170
is included for each type of floating point
exception. If the mask bit is set,
then the exception is disabled. If the
mask bit is clear, the exception is
enabled.

Detailed Description Text - DETX (83):
    In accordance with the above disclosure,
a floating point unit has been
shown which conveys the **rounding** mode
corresponding to a particular instruction
with that particular instruction into the
execution pipeline. The **rounding**
mode is updated as control word update
instructions are dispatched, such that
subsequent instructions receive the updated
rounding mode. Advantageously, the
control word update instruction may be
performed in a non-serialized manner if
the only update is to the **rounding** mode.
If other portions of the control word
are updated, the instructions subsequent to

the control word update instruction
may be discarded and refetched.
Performance of those applications which
change
the **rounding** mode often may advantageously
be increased.

Claims Text - CLTX (3):
    a **rounding** mode storage circuit coupled
to said execution pipeline

Claims Text - CLTX (4):
    a control word storage circuit coupled
to the **rounding** mode storage circuit;

Claims Text - CLTX (5):
    wherein said **rounding** mode storage
circuit and said control word storage
circuit are configured to store a **rounding**
mode indicative of a type of
rounding to be applied to results of
floating point instructions;

Claims Text - CLTX (6):
    a control unit circuit coupled to said
rounding mode storage circuit,
wherein said control unit circuit is
configured to detect a dispatched control
word update instruction, and wherein said
control unit circuit is configured to
update said **rounding** mode storage circuit

with an updated **rounding** mode in
response to said control unit circuit
detecting the dispatched control word
update instruction, wherein said control
unit circuit updates said **rounding**
mode storage circuit prior to execution of
the dispatched control word update
instruction;

Claims Text - CLTX (7):
   wherein said execution pipeline is
configured to receive said updated
rounding mode along with a particular
instruction as said particular
instruction is dispatched into said
execution pipeline, and wherein the
execution pipeline is further configured to
round a particular result
corresponding to said particular
instruction according to said updated
rounding
mode;

Claims Text - CLTX (8):
   wherein the control word storage circuit
is configured to be updated with
the updated **rounding** mode after execution
of the dispatched control word update
instruction.

Claims Text - CLTX (9):
   2. The floating point unit as recited

·in claim 1 wherein said execution
pipeline comprises a **rounding** stage at
which **rounding** is performed, wherein
said **rounding** stage is coupled to receive
said **rounding** mode and to **round** said
particular result accordingly.

Claims Text - CLTX (10):
   3. The floating point unit as recited
in claim 2 wherein said **rounding**
stage is configured to perform only said
rounding.

Claims Text - CLTX (12):
   5. The floating point unit as recited
in claim 4 wherein said assembly
queue includes said **rounding** mode storage.

Claims Text - CLTX (14):
   7. The floating point unit as recited
in claim 6 wherein said **rounding** mode
storage is updated with a **rounding** mode
portion of said updated control word.

Claims Text - CLTX (17):
   10. The floating point unit as recited
in claim 9 wherein said **rounding**
mode storage is coupled to said control
word register, and wherein said control
unit is configured to cause said **rounding**
mode storage to store a **rounding** mode

`portion of said current control word upon
receiving said indication.

Claims Text - CLTX (19):
    a floating point unit including an
execution pipeline, wherein said floating
point unit is configured to convey a
rounding mode stored in a first **rounding**
mode storage circuit along with each
instruction into said execution pipeline,
wherein said floating point unit is
configured to update said **rounding** mode
stored in a first **rounding** mode storage
circuit with an updated **rounding** mode
in response to dispatching a control word
update instruction, and wherein said
floating point unit is configured to update
a second **rounding** mode storage
circuit with the updated **rounding** mode in
response to execution of the control
word update instruction;   and

Claims Text - CLTX (21):
    12.   The microprocessor as recited in
claim 11 wherein said floating point
unit is configured to update said first
rounding mode storage circuit before a
second **rounding** mode stored in second
storage circuit before the second storage
circuit is updated with the updated
rounding mode if said cancel indication is
received from said reorder buffer.

Claims Text - CLTX (22):
    13. A method for performing **rounding** in
a floating point unit comprising:

Claims Text - CLTX (23):
    storing a current **rounding** mode in a
first storage circuit;

Claims Text - CLTX (24):
    storing the current **rounding** mode in a
second storage circuit;

Claims Text - CLTX (25):
    conveying the current **rounding** mode
stored in the first storage circuit
along with a floating point instruction
into an execution pipeline of said
floating point unit;   and

Claims Text - CLTX (26):
    updating said first storage circuit with
an updated **rounding** mode upon
dispatch of a control word update
instruction into said execution pipeline,
wherein said updating occurs before
execution of the control word update
instruction;

Claims Text - CLTX (27):

updating said second storage circuit with said updated **rounding** mode after execution of the control word update instruction.

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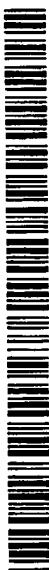
(54) Title: APPARATUS AND METHOD FOR REDUCING ARTIFACTS PRESENT IN A LINE SCANNED VIDEO DISPLAY

(57) Abstract: On a line scanned video display, the frequency of an artifact producing signal within the video passband is selected to be an odd harmonic of one half the horizontal line scan frequency so that adjacent scan lines of the artifact are 180 degrees out of phase with each other. Thus, the artifact is rendered largely visually canceled when viewed due to the integrating characteristics of the eye of the viewer, even though the artifact is still there.

APPARATUS AND METHOD FOR REDUCING ARTIFACTS PRESENT IN A LINE SCANNED VIDEO DISPLAY

FIELD OF THE INVENTION

5   The present invention relates to the processing of video signals, and more particularly, to the amelioration of artifacts introduced by periodic signals leaking or introduced into the luminance channel of a color television receiver.

BACKGROUND

10   As a review, for an NTSC color television signal, the spectral energy of the luminance (Y) signal is essentially centered at harmonics of the line scanning frequency nf_h where n is an integer. Thus, a luminance signal typically has frequency components of $1f_h$, $2f_h$, $3f_h$, $4f_h$, etc. The chrominance (C) signal spectral energy peaks occur at odd harmonics of one half the line scanning frequency, i.e.,

15      $(n+1/2)f_h$ where n is an integer. Thus, the Y and C energy spectra are frequency interleaved.

        U.S. Patent No. 4,607,286 of Weimer concerns the electrostatic coupling of forward clocking signals in a CCD imager to the underlying bulk semiconductor substrate which introduces transient disturbances leaving visible

20   artifacts in television pictures reconstructed from the video signals generated from the CCD imager. An additional clocked delay places the disturbances into the line retrace interval and the disturbances are removed from the video signals by line retrace blanking.

        U.S Patent Nos. 4,291,330 and 4,134,126, both of Hirai, teach that in a

25   color video recorder, an interfering or cross-talk signal having a frequency $(n+1/2)f_h$ will have a frequency interleaved relationship to the frequency of the main luminance components with the result that the cross-talk signal will be phase inverted in successive horizontal lines of the video signals, and that since there is a high correlation between the reproduced luminance components in successive horizontal

30   line intervals, the cross-talk signals will not appear as a conspicuous noise or beat on an image reproduced on a cathode ray tube but will be largely visually canceled.

        U.S. Patent No. 4,003,077 of Hickock concerns a color video recorder wherein the chrominance information is frequency converted before recording to a frequency to render, upon display, an artifact pattern of one line of the picture frame

35   being 180 degrees out of phase with the artifact pattern of an adjacent line, so that the resultant artifact pattern, although present, seemingly disappears due to the integrating effect of the eye of the viewer.

SUMMARY OF THE INVENTION

During production of a video processing integrated circuit having, inter alia, a graphics generator, a video processor, and a spread spectrum clock, it was discovered that the signal for FM modulating the carrier signal of the clock, due to

5   internal signal leakage within the chip, caused an artifact to appear when viewed on a line scanned video display, e.g., a cathode ray tube. Rather than undertake the extensive and expensive redesign of the integrated circuit to eliminate the artifact, since the frequency of the interfering signal was selectable, it was decided to select the frequency of the interfering signal so that the frequency would be an odd

10   harmonic of one half the horizontal line scan frequency. By making the particular selection of frequency to be an odd harmonic of one half of the horizontal line scan frequency, adjacent scan lines of the artifact are 180 degrees out of phase with each other. Thus, the artifact is rendered largely visually canceled when viewed on a line scanned display, due to the integrating characteristics of the eye of the viewer, even

15   though the artifact is still there.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The exemplary embodiment of the present invention concerns an integrated circuit number W49C31-20A which is a low-power CMOS monolithic chip

20   made by the IC Works of San Jose, California, USA, and includes a graphics processor, a video processor and a spread spectrum clock. The present invention concerns a video processor wherein a signal having a frequency within the video passband "leaks" into the video processor, and in the exemplary embodiment, the leaked signal, which produces an artifact on a video display, is derived from the

25   modulation signal of a spread spectrum clock. It should be noted however, for purposes of the present invention, that the leaked artifact producing signal can be derived from any source, and leaked or introduced into any common video processor. Thus, the construction and circuitry of the exemplary chip including the exemplary video processor, the exemplary spread spectrum clock, and the

30   exemplary generation of the modulation signal for the spread spectrum clock, all form no part of the present invention.

It is believed that the artifact creating signal leaks into the video path by electrostatic and/or capacitive coupling either between sections, or through electrostatic and/or capacitive coupling by the respective structures with the

35   semiconductor substrate material. The artifact creating signal in the exemplary embodiment, is the modulation signal of a spread spectrum clock which falls within the video passband of up to 10 MHz. The carrier signal for the clock is outside of the video passband, i.e., 85 MHz, but if it fell within the video passband, or any other

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frequency selectable, periodic, artifact producing signal fell within the video passband, the present invention would be equally applicable in order to "hide" the produced artifact.

More particularly, during production of the monolithic integrated circuit it 5 was discovered that the signal for FM modulating the carrier signal of the clock, due to internal signal leakage within the chip, caused an artifact to appear when viewed on a line scanned video display such as a cathode ray tube. Rather than undertake the extensive and expensive redesign of the integrated circuit to eliminate the artifact, it was decided to take an alternate approach.

10 The frequency of the interfering signal was selectable. Thus, it was decided that since the frequency was selectable, to select the frequency of the interfering signal so that the signal frequency would be an odd harmonic of one half the horizontal line scan frequency commonly referred to as f_h, which for an NTSC signal is 15,734.26573 Hz. Thus, the particular selection of frequency of the 15 interfering modulation signal of the spread spectrum clock was 39.336 kHz (2.5 multiplied by f_h), which can be rounded up or down to the nearest integral kHz of 39 kHz or 40 kHz.

For such a harmonic relationship to f_h, the artifact displayed on adjacent scan lines on the line scanned display are 180 degrees out of phase with 20 each other. Thus, the artifact is rendered largely visually canceled when viewed due to the integrating characteristics of the eye of the viewer, even though the artifact is still there. This is true for both interlaced and progressive scan frames except that one line at the top or bottom of each interlace field will not appear to be canceled. The line having the visually unreduced artifact can be placed in the vertical overscan 25 portion of picture, and thus will be hidden, or can be hidden by vertical blanking.

Further, the interfering signal is also frequency interleaved with the luminance signal, as discussed above in the background section. The frequency interleaving further reduces artifacts.

The present invention is applicable to the choice of the frequency of a 30 periodic signal within the video passband, leaked or intentionally introduced by whatever means, into a video signal path of whatever means, which causes an artifact to appear when viewed on a line scanned display. Such an intentional introduction of an artifact producing signal into the video path can be, e.g., an information encoded signal. It should be noted that the artifact producing signal of 35 the exemplary embodiment is an information encoded signal but the introduction into the video signal path was unintentional.

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CLAIMS

1. In a television receiver having a line scanned video display, a method for reducing the visual effects of an artifact in a line scan portion of the video signal display, the artifact being attributable to a periodic signal within the video pass band coupled to a video processing path of a video circuit, the line scan having a frequency of f_h, comprising:

selecting the frequency of the periodic signal, and

predetermining the frequency of the periodic signal to be an odd harmonic of $f_h/2$.

2. The method of claim 1 wherein the periodic signal is a clock signal electrostatically/capacitively coupled to the video circuit.

3. The method of claim 2 wherein the electrostatically/capacitively coupled clock signal is an FM modulating signal of a spread spectrum clock.

4. The method of claim 2 wherein the electrostatically/capacitively coupled clock signal is a carrier signal of a spread spectrum clock.

5. The method of claim 1 wherein f_h is the NTSC standard horizontal scan frequency of 15,734.26573 Hz and the predetermined fundamental frequency of the periodic signal is approximately 39.336 kHz (2.5 multiplied by f_h).

6. The method of claim 5 wherein the predetermined fundamental frequency of the periodic signal is rounded up or rounded down to an integral number.

7. The method of claim 1 wherein the predetermined fundamental frequency of the periodic signal is one of rounded up and rounded down to an integral number.

8. The method of claim 2 wherein the video circuit, and the electrostatically/capacitively coupled periodic signal are included within an integrated circuit having an underlying substrate of semiconductor material.

9. The method of claim 8 wherein the electrostatically/capacitively coupling is via respective capacitances coupled to the underlying substrate.

10. The method of claim 1 wherein the periodic signal is electrostatically/capacitively coupled to the video circuit.

11. The method of claim 10 wherein the video circuit, and the electrostatically/capacitively coupled periodic signal are included within a monolithic integrated circuit having an underlying substrate of semiconductor material.

12. The method of claim 11 wherein the electrostatic coupling is via capacitances to one of the underlying substrate and between component parts of the monolithic integrated circuit.

13. In a television receiver having a line scanned video display, apparatus for reducing the visual effects of an artifact in a line scan portion of the video signal display, the artifact being attributable to a periodic signal within the video passband coupled to a video processing path of a video circuit, the line scan having a frequency of f_h, comprising:

means for selecting the frequency of the periodic signal, and

means for predetermining the frequency of the periodic signal to be an odd harmonic of $f_h/2$.

14. The apparatus of claim 13 wherein the periodic signal is a clock signal electrostatically/capacitively coupled to the video circuit.

15. The apparatus of claim 14 wherein the electrostatically/capacitively coupled clock signal is an FM modulating signal of a spread spectrum clock.

16. The apparatus of claim 14 wherein the electrostatically/capacitively coupled clock signal is a carrier signal of a spread spectrum clock.

17. The apparatus of claim 13 wherein f_h is the NTSC standard horizontal scan frequency of 15,734.26573 Hz and the predetermined fundamental frequency of the periodic signal is approximately 39.336 kHz (2.5 multiplied by f_h).

18. The apparatus of claim 17 wherein the predetermined fundamental frequency of the periodic signal is one of rounded up and rounded down to an integral number.

19. The apparatus of claim 13 wherein the predetermined fundamental frequency of the periodic signal is rounded up or rounded down to an integral number.

20. The apparatus of claim 14 wherein the video circuit, and the electrostatically/capacitively coupled periodic signal are included within an integrated circuit having an underlying substrate of semiconductor material.

21. The apparatus of claim 20 wherein the electrostatically/capacitively coupling is via respective capacitances coupled to the underlying substrate.

22. The apparatus of claim 13 wherein the periodic signal is electrostatically/capacitively coupled to the video circuit.

23. The apparatus of claim 22 wherein the video circuit, and the electrostatically/capacitively coupled periodic signal are included within a monolithic integrated circuit having an underlying substrate of semiconductor material.

24. The apparatus of claim 23 wherein the electrostatically/capacitively coupling is via capacitances to one of the underlying substrate and directly between component parts of the monolithic integrated circuit.

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7   H04N5/44   H04N5/21

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7   H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

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X	US 5 596 418 A (YUN JONG K ET AL) 21 January 1997 (1997-01-21) column 12, line 12 –column 55, line 45 ---	1,13
Y	US 5 461 426 A (PATEL CHANDRAKANT B ET AL) 24 October 1995 (1995-10-24) column 8, line 37 –column 42, line 22 ---	8-12, 20-24
Y	US 4 607 286 A (WEIMER PAUL K) 19 August 1986 (1986-08-19) cited in the application column 3, line 22 –column 10, line 33 ---	8-12, 20-24

-/-

X	Further documents are listed in the continuation of box C.		X	Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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